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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 12

Application Number: 09/989,563
Filing Date: November 19, 2001
Appellant(s): SHER ET AL.

Jerry T. Sewell
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed January 10, 2003.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The brief does not contain a statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief. Therefore, it is presumed that there are none. The Board, however, may exercise its discretion to require an explicit statement as to the existence of any related appeals and interferences.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct. However, the rejection of claims 22-24 has been withdrawn.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 1-9, 15, 16 and 25; 10-14 and 17-24 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,483,486	Javanifard et al.	01-1996
5,473,277	Furumochi	12-1995

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Javaniferd et al. (USP 5483486, Applicant submitted IDS) in view of Furumochi (USP 5473277, Applicant submitted IDS).

As to claim 1, Javanifrad et al. shows in figure 14 a voltage control circuit, which provides a test supply voltage (VOUT), comprising: a reference circuit (316); a voltage regulator (318) electrically coupled to the reference circuit which generates a first control signal (REG); a charge pump (320) which receives the control signal from the voltage regulator, the charge pump generating the test supply voltage (VOUT). Thus, figure 14 shows all limitations of claim 1 except for the reference circuit (316) having a plurality of voltage regulation devices and at least one bypass device connected to at least one of the plurality of voltage regulation devices. However, it is notorious well known in the art that Javanifrad's test supply voltage (VOUT) is determined by the reference voltage (VREF). An adjustable test supply voltage (VOUT) will

provide more flexible for the voltage control circuit to generating desired test supply voltage (VOUT). Furumochi's figure 5 shows a reference circuit having plurality of voltage regulation devices (T1-T4) and at least one bypass device (SW0(TN4)) connected to at least one of the plurality of voltage regulation devices. Furumochi's circuit having an advantage of providing an adjustable reference voltage at the output node (OUT). Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to modify Javaniard'et al.'s voltage control circuit by using a reference circuit as taught by Furumochi for the purpose of generating an adjustable reference voltage. The skilled in the art would have been motivated to use the adjustable reference voltage to generate an adjustable test supply voltage (VOUT). Therefore, the modified Javanifrad et al. circuit shows the at least one bypass device [Furumochi's SW0(TN4) or (circuit 14 and SW0(TN4)] is activated following the certification of the semiconductor device to bypass the at least one of the plurality of voltage regulation devices from the clamp circuit to lower the clamping threshold of the clamp circuit, the voltage regulator generating a second control signal responsive to the lowered clamping threshold of the clamp circuit to cause the charge pump to generate the operational supply voltage, as called for in claim 1.

As to claim 2, the modified Javanifrad et al. circuit shows the plurality of voltage regulation devices (Furumochi's T1-T4) comprise diodes.

As to claim 3, the modified Javanifrad et al. circuit shows the diodes (Furumochi's T1-T4) are implemented through transistors.

As to claim 4, the modified Javanifrad et al. circuit further shows the bypass device comprising a fuse (Furumochi's FU) in series with a transistor (TN4).

As to claim 5, the modified Javanifrad et al. circuit shows bypass device is activated by blowing the fuse.

As to claim 6, the modified Javanifrad et al. circuit shows the value of the operational supply voltage is reduced for each voltage regulation device bypassed.

As to claim 7, the modified Javanifrad et al. circuit shows the voltage regulation devices (Furomocho's T1-T4) limit the maximum voltage output of the clamp circuit.

As to claim 8, the modified Javanifrad et al. circuit shows the first control signal reduces the test supply voltage (VOUT) when the voltage regulation devices (Furomocho's T1-T4) limit the output of the clamp circuit.

As to claim 9, the modified Javanifrad et al. circuit shows the second control signal reduces the operational supply voltage when the non-bypassed voltage regulation devices (T1, T2..) limit the output of the clamp circuit.

As to claim 10, Javanifrad et al. shows in figure 14 a voltage control circuit, which provides a test supply voltage (VOUT), comprising: means (316) for providing reference voltage (VREF); means (318) for generating a first control signal (REG) based upon the output of the means for providing the reference voltage; means (320) for generating the test supply voltage (VOUT). Thus, figure 14 shows all limitations of claim 10 except for the means for providing reference voltage (316) having a clamp circuit, means for controlling an output of a clamp circuit, and means for limiting the output of the clamp circuit. However, it is notorious well known in the art that Javanifrad's test supply voltage (VOUT) is determined by the reference voltage (VREF). An adjustable test supply voltage (VOUT) will provide more flexible for the voltage control circuit to generating desired test supply voltage (VOUT). Furumochi's figure 5

shows a reference circuit having a clamp circuit (RL, T1-T4) and means (T1-T4) for controlling an output of the clamp circuit, and means (SW0(TN4) or (circuit 14 and SW0(TN4)) for limiting the output of the clamp circuit. Furumochi's circuit having an advantage of providing an adjustable reference voltage at the output node (OUT). Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to modify Javaniard et al.'s voltage control circuit by using a reference circuit as taught by Furumochi for the purpose of generating an adjustable reference voltage. The skilled in the art would have been motivated t use the adjustable reference voltage to generate an adjustable test supply voltage (VOUT). Therefore, the modified Javanifrad et al. circuit shows means (Furumochi's T1-T4) for controlling an output of a clamp circuit (Furumochi's RL, T1-T4); means (Furumochi's (SW0(TN4)) for limiting the output of the clamp circuit, means Javanifard et al.'s (318) for generating a second control signal base upon the limited output of the clamp circuit (the means for generating a first control signal and means for generating a second control signal are the same as shown in Applicant's figure 2 (means 220)); and means (Javanifard et al.'s 320) for generating the operational supply voltage (the means for generating test supply voltage and means for generating the operation test supply voltage are the same as shown in Application's figure 1 (means 120), as called in for claim 10.

As to claim 11, the modified Javanifrad et al. circuit shows the control means comprises diodes (Furumochi's figure 5).

As to claim 12, the modified Javanifrad et al. circuit shows the diodes are implemented through transistors (Furumochi's figure 5).

As to claim 13, the modified Javanifrad et al. circuit shows the limiting means comprising a fuse (FU) (Furumochi's figure 5).

As to claim 14, the modified Javanifrad et al. circuit shows the limiting means comprises a transistor [SW0(TN4)] (Furumochi's figure 5).

As to claim 15, Javanifrad et al. shows in figure 14 a voltage control circuit, which provides a test supply voltage (VOUT), comprising: a reference circuit (316); a voltage regulator (318) electrically coupled to the reference circuit which generates a first control signal (REG); a charge pump (320) which receives the control signal from the voltage regulator, the charge pump generating the test supply voltage (VOUT). Thus, figure 14 shows all limitations of claim 15 except for the reference circuit (316) having a clamp circuit, a plurality of voltage regulation devices, and at least one bypass device connected to at least one of the plurality of voltage regulation devices. However, it is notorious well known in the art that Javanifrad's test supply voltage (VOUT) is determined by the reference voltage (VREF). An adjustable test supply voltage (VOUT) will provide more flexible for the voltage control circuit to generating desired test supply voltage (VOUT). Furumochi's figure 5 shows a reference circuit having a clamp circuit (RL, T1-T4) and means (T1-T4) for controlling an output of the clamp circuit, and means (SW0(TN4) or (circuit 14 and SW0(TN4)) for limiting the output of the clamp circuit. Furumochi's circuit having an advantage of providing an adjustable reference voltage at the output node (OUT). Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to modify Javaniard et al.'s voltage control circuit by using a reference circuit as taught by Furumochi for the purpose of generating an adjustable reference voltage. The skilled in the art would have been motivated t use the adjustable reference voltage

to generate an adjustable test supply voltage (VOUT). Therefore, the modified Javanifrad further shows a clamp (Furumochi's RL, T1-T4) circuit having a plurality of voltage regulation devices (T1-T4), the voltage regulation devices controlling a clamping threshold of the clamp circuit; at least one bypass device (Furumochi's SW0(TN4) or (circuit 14 and SW0(TN4)) connected to at least one of the plurality of voltage regulation devices, wherein the at least one bypass device is reversibly activated (when the input of transistor TN4 is high, the transistor (TN4) is reversibly activated (the output of transistor is low)). to reversibly by pass (the current from transistor T4 is reversibly going to through transistor TN4) the at least one of the plurality of voltage regulation devices from the clamp circuit, thereby modifying the claming threshold of the clamp circuit.

As to claim 16, the modified Javanifard et al. circuit shows the bypass device comprises a fuse (Furumochi's FU) in series with a control terminal of a transistor [SW0(TN4)].

As to claim 17, Javanifard et al. figure 14 shows a method for providing a supply voltage comprising: establishing a voltage control signal (VREF) from a reference voltage generator (316); generating a supply voltage (VOUT). Thus, figure 14 shows all limitations of claim 17 except for the reference voltage generator comprising plurality of voltage control elements and a bypass device for reversibly by pass at least one of the plurality of the voltage control elements. However, it is notorious well known in the art that Javanifrad's test supply voltage (VOUT) is determined by the reference voltage (VREF). An adjustable test supply voltage (VOUT) will provide more flexible for the voltage control circuit to generating desired test supply voltage (VOUT). Furumochi's figure 5 shows a reference circuit having a clamp circuit (RL, T1-T4) and means (T1-T4) for controlling an output of the clamp circuit, and means (SW0(TN4) or (circuit 14 and SW0(TN4)) for limiting the output of the clamp circuit. Furumochi's circuit

having an advantage of providing an adjustable reference voltage at the output node (OUT). Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to modify Javaniard et al.'s voltage control circuit by using a reference circuit as taught by Furumochi for the purpose of generating an adjustable reference voltage. The skilled in the art would have been motivated t use the adjustable reference voltage to generate an adjustable test supply voltage (VOUT). Therefore, the modified Javanifrad et al.'s shows a method comprising the step of the providing plurality voltage control elements (Furumochi's T1-T4); establishing a first voltage control signal (Furumochi's OUT) from the voltage control elements; generating the first supply voltage (Javanifard et al.'s VOUT) from the first voltage control signal; reversibly bypassing (the current from transistor T4 is reversibly going to through transistor TN4) at least one (Furumochi's T4) of the plurality of voltage control elements; establishing a second voltage control signal (Furumochi;s OUT) from the plurality of voltage control elements which are not reversibly bypassed; and generating the second supply voltage (Javanifard et al.'s VOUT) from the second voltage control signal.

As to claim 18, the modified Javanifard et al.circuit shows the first supply voltage has a voltage magnitude greater than the second supply voltage (when Furumochi's transistor T4 is bypassed, the output voltage (OUT) is less than the original voltage. Therefore, Javanifard et al.'s second supply voltage (VOUT) is less than the first supply voltage).

As to claim 19, the modified Javanifard et al. circuit shows the plurality of voltage control elements (Furomocho's T1-T4) comprise diodes.

As to claim 20 the modified Javanifard et al.' circuit shows reversibly bypassing at least one of the plurality of voltage control elements comprises applying a control signal to a bypass device (Furumochi's SW0(NT4)).

As to claim 21, the modified Javanifard et al. circuit shows the first supply voltage and the second supply voltage are generated by a charge pump (320).

As to claim 25, Javanifrad et al. shows in figure 14 a voltage control circuit, which provides an internal supply voltage (VOUT), the internal supply voltage derived from an external supply voltage (Vin) that varies over a range of magnitudes, the voltage control circuit comprising: a reference circuit (316); a voltage regulator (318) electrically coupled to the reference circuit which generates a first control signal (REG); a charge pump (320) which receives the control signal from the voltage regulator, the charge pump generating the internal supply voltage (VOUT). Thus, figure 14 shows all limitations of claim 1 except for the reference circuit (316) having a plurality of voltage regulation devices and at least one bypass device connected to at least one of the plurality of voltage regulation devices. However, it is notorious well known in the art that Javanifrad's test supply voltage (VOUT) is determined by the reference voltage (VREF). An adjustable test supply voltage (VOUT) will provide more flexible for the voltage control circuit to generating desired test supply voltage (VOUT). Furumochi's figure 5 shows a reference circuit having a clamp circuit (RL, T1-T4) and means (T1-T4) for controlling an output of the clamp circuit, and means (SW0(TN4) or (circuit 14 and SW0(TN4)) for limiting the output of the clamp circuit. Furumochi's circuit having an advantage of providing an adjustable reference voltage at the output node (OUT). Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to modify

Javaniard et al.'s voltage control circuit by using a reference circuit as taught by Furumochi for the purpose of generating an adjustable reference voltage. The skilled in the art would have been motivated t use the adjustable reference voltage to generate an adjustable test supply voltage (VOUT). Therefore, the modified Javanifrad further shows the at least one bypass device (Furumochi's SW0(TN4) or (circuit 14 and SW0(TN4)) is activated following the certification of the semiconductor device to bypass the at least one of the plurality of voltage regulation devices from the clamp circuit to lower the clamping threshold of the clamp circuit, the voltage regulator generating a second control signal responsive to the lowered clamping threshold of the clamp circuit to cause the charge pump to generate the internal supply voltage at an operational magnitude having a reduced differential magnitude with respect to magnitude of the external supply voltage.

(11) Response to Argument

Appellant's arguments have been fully considered but they are not persuasive.

The Examiner agrees with the statements regarding to the operations of Javanifard et al. and Furumochi in page 4.

Group II, claims 1-9, 15, 16 and 25

Appellant argues that neither the Javanifrad et al. reference nor the Furumochi reference teaches or suggests a voltage control circuit comprising a clamp circuit having a clamp threshold. The Examiner respectfully disagrees. It is well known in the art that a diode will perform a clamping function. Appellant acknowledges this function in page 9 of the appeal brief. Furumochi's figure 5 shows a reference voltage generation circuit having plurality of diodes (T1-T4) connected in series. The diodes T1-T4 will perform a clamping function and limit the output

voltage (OUT) to be at a level equal to the total threshold of the diodes T1-T4. Thus, Furumochi's circuit figure 5 can be see to act as a clamp circuit by forcing and limiting the output voltage.

Appellant further argues that Furumochi describes a constant voltage generator as being designed for supplying a constant voltage with strict precision (see column 7, lines 16-17). The voltage supplied by the Furumochi circuit is kept fixed, as noted by the Examiner, and not allowed to vary above or below the voltage selected by diode-configured transistors that are not bypassed. To assert that Furumochi teaches or suggests a clamp circuit not only goes against the accepting meaning of the term, but also ignores other express limitations of claim 1, including the limitation of a clamping threshold. The Examiner respectfully disagrees. The diodes of Furumochi will perform as a clamp circuit and will limit the voltage at the output to the threshold of the diodes. This inherent function of a diode does not require a variable supply signal. It is not necessary for the supply signal to be varied in order for the diodes operate as a clamp circuit. Furumochi's diodes T1-T4 force the output voltage to be at the total threshold (clamp threshold) of the diodes independent of the supply voltage. Thus, Furumochi's figure 5 in combination with Javanifard, discloses a clamp circuit (Furumochi's figure 5) with a clamp threshold (the total threshold of the un-bypassed diodes (T1-T4).

Appellant further argues that neither Javanifard nor Furumochi recites a voltage control circuit that comprises a bypass device that is activated following the certification of a semiconductor device to bypass at least one of the plurality of voltage regulation devices to lower clamping threshold of the clamp circuit. The Examiner respectfully disagrees. Furumochi's Figure 5 shows the switching element [SW0(TN4)] (bypass device) connected in

parallel with diode T4. When the input of switch [SW0(TN4)] is high, transistor TN4 will turned ON and bypass diode T4. The clamp circuit Figure 5 will provide an output voltage (OUT) equal to the total threshold (clamp threshold) of diodes T1-T3. This output voltage level is lower than the output voltage VOUT before diode T4 is bypassed.

Appealant argues that there is no suggestion or motivation to combine or modify the references that would make Claim 1 obvious to one ordinary skill in the art. The rejection of claim 1 clearly providing motivation to combine the references. That motivation is having more flexibility to provide a desired test voltage when using an adjustable reference circuit.

Appellant states that even though Furumochi discloses the use of diode-configured transistors in its voltage reference circuit depicted in Figure 5, Furumochi never discloses or suggests a clamp circuit having clamping threshold. The Examiner disagrees. The Fufumochi's diodes T1-T4 force the output voltage to be at total threshold of the diodes. Therefore, the circuit figure 5 is a clamp circuit, wherein the total threshold of the diodes is the clamp threshold of the clamp circuit Figure 5.

Group II, claims 10-14

Appellant argues that clamp 10 is an apparatus claim defined with mean plus function limitations... Claims 11-14 must be examined in accordance with the guidelines set for in M.P.E.P. §§ 2181-2186. The Examiner respectfully disagrees. Furumochi Figure 5 having similar structure with Appellant clamping circuit in Figure 4A. Both circuits having resistor in series with plurality of diodes, and both circuits having bypass element for bypassing at least one diode. Thus, Furumochi's having equivalent function with Applicant's clamp circuit. Therefore, the combination of Javanifrad and Furumochi shows a circuit having elements equivalent with

the elements in clam 10. Therefore, the rejection of claim 10 is proper according to M.P.E.P §§ 2181-2186.

Appellants further state that there is no suggestion in either reference of a means for generating a first control signal based upon the output of the clamp circuit, means for generating a second control signal, and means for generating an operation supply voltage. The Examiner respectfully disagrees. According to Figures 1-5 of the subject application, circuit 210 generates a first control signal before one of the diode is bypassed. Circuit 210 also generates a second control signal after one of the diode is bypassed. Thus, the means for generating first and second control signal in claim 10 are a single circuit element in the Appellants' circuit . The means for generating the test supply voltage and means for generating the operation supply voltage are also a single circuit element. Furumochi discloses a reference circuit having clamp circuit (diodes T1-T4). Furumochi's figure 5 generates a first control signal based upon the output of the clamp circuit (T1-T4). After transistor T4 is bypass, Furumochi Figure 5 generates a second control signal lower than the first control signal. Thus, Furumochi Figure 5 comprises first and second means for generating first and second control signals. Javanifard's charge pump circuit generating first and second test supply voltages in response to the first and second control signals. As subject invention is understood from Appellants's figures 1-5, the combination of Javanifard and Furumochi shows all limitations of claim 10.

Group III, claims 17-24

Appellants state that Furumochi does not teach or suggest a method comprising the step of reversible bypassing at least one of a plurality of voltage control element. The Examiner respectfully disagrees. The subject specification does not define the term "reversibly". In The

Original Roget's Thesaurus of English Words and Phrases dictionary, "reversibly" is defined as meaning backwards. Reversibly bypass is broadly interpreted as a bypass function in which the current in the circuit changes direction. In Furumochi's figure 5, when the in put of transistor [SW0(TN4)] is high, the current in the diode T4 will change direction to ground via transistor [SW0(TN4)]. Therefore, figure 5 shows the step of reversibly bypassing at least one of a plurality of voltage control elements.

The rejection of claims 22-24 has been withdrawn.

(12) Conclusion

The Examiner respectfully submits that the combination of Javanifard's circuit and Furumochi's circuit shows all limitations of the rejected claims. Therefore, the rejections should be sustained.

Respectfully submitted,

QT
March 24, 2003

Conferees

- Timothy Callahan
- Olik Chaudhuri
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